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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/643,967	08/20/2003	Hiroyuki Nansei	030993	4992

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EXAMINER	
THOMAS, TONIAE M	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 04/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/643,967	NANSEI ET AL.
	Examiner	Art Unit
	Toniae M. Thomas	2822

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-40* is/are pending in the application.

4a) Of the above claim(s) *12-38* is/are withdrawn from consideration.

5)☒ Claim(s) *3,4,8,9,39 and 40* is/are allowed.

6)☒ Claim(s) *1 and 5* is/are rejected.

7)☒ Claim(s) *6,7,10 and 11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 04 April 2005 has been entered.

2. The amendment filed on 04 April 2005 cancelled claim 2. Accordingly, claims 1 and 3-40 are currently pending. Of these, claims 12-29 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected species, and claims 30-38 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention.

Allowability Withdrawn

3. In the final Office action mailed on 02 December 2004, claim 2 was indicated as being allowable over the prior art of record. Likewise, claim 5, which depended from claim 2, was also indicated as being allowable because it depended from claim 2. Accordingly, Applicant cancelled claim 2, amended claim 1 to include the limitations of claim 2, and amended claim 5 to depend from claim 1. However, the indicated allowability of claims 2 and 5 is

withdrawn in view of the newly discovered reference to *Yang et al. (US 6,479,402 B1)*. Rejections based on the newly cited reference follow.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dobuzinsky et al. (US 5,330,935) in view of Weimer (US 2003/0040171 A1) and Chua et al. (US 2004/0038486 A1.[1]

The Dobuzinsky et al. patent (Dobuzinsky) teaches a method for forming a thin film on a semiconductor device (fig. 5B and col. 6, lines 38-64). The method comprises the steps of: forming a lower silicon oxide film 39(fig. 5B and col. 6, lines 54-55); forming a silicon nitride film 40 on the lower silicon oxide film (fig. 5B and col. 6, lines 56-57), wherein a multilayered insulating film including at least the lower silicon oxide film and the silicon nitride film is formed (fig. 5B and col. 6, lines 54-57); and forming an upper silicon oxide film 41 on the silicon nitride film using a plasma oxidizing method (fig. 5B and col.

[1] The Weimer and Chua et al. references were relied upon in the previous Office action.

6, lines 38-50 and col. 6, lines 58-59), wherein a multilayered insulating film composed of the lower silicon oxide film, the silicon nitride film, and the upper silicon oxide film is formed (fig. 5B and col. 6, lines 54-59).

Dobuzinsky lacks anticipation of forming the silicon nitride layer by the following method: forming a silicon film on the lower silicon oxide film, and completely nitriding the silicon film with a surface wave plasma generated by a plasma nitriding method.

The Weimer US pre-grant published application (Weimer) discloses a method for manufacturing a semiconductor device, the semiconductor device comprising a multilayered insulating film including a silicon oxide film having a silicon nitride film formed thereon (figs. 1-4 and accompanying text). The silicon nitride film is formed as follows: a lower silicon oxide film 16 is formed (fig. 1 and par. 23, lines 6-7); a silicon film 18 is on the lower silicon oxide film (fig. 2 and par. 24, lines 1-5); and, using a plasma nitriding method, the silicon film is completely nitrided to form a silicon nitride film 20 on the lower silicon oxide film 16 (fig. 3; par. 26, lines 1-10; and par. 28, lines 1-12).

Again, Weimer teaches using a plasma nitriding method to completely nitride the silicon film. Weimer further teaches plasma nitriding the silicon film using an ICP system, an ECR system, or other plasma nitriding systems (par. 008, lines 21-25). While Weimer teaches plasma nitriding the silicon film using an ICP system, an ECR system, or other plasma nitriding systems,

Weimer does not teach that the nitriding is done with a surface wave-plasma generated by a plasma nitriding method.

The Chua et al. pre-grant published application (Chua) discloses a method for forming a nitride layer using a plasma nitriding method (par. 0061). The plasma nitriding method is selected from one of an ICP system, a radial line slot antenna system, an ECR system, etc. (par. 0061). The radial line slot antenna system is a plasma nitriding method that generates a surface wave-plasma.

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify Dobuzinsky by forming the silicon nitride layer using the method of Weimer, because the resulting silicon nitride is thinner than a silicon nitride layer formed by conventional deposition methods (Weimer – par. 5, lines 7-14). This, in turn, reduces the total thickness of the silicon oxide/silicon nitride/silicon oxide (ONO) multilayered insulating film. In addition, it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to nitridize the silicon film using a radial line slot antenna system, as taught by Chua, because plasma nitriding using a radial line slot antenna system is well known in the art.

5. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dobuzinsky in view of Weimer and Chua as

applied to claim 1 above, and further in view of Maita et al. (US 5,861,347).

As discussed above, the method of Dobuzinsky forms a multilayered insulating film composed of a lower silicon oxide film, a silicon nitride film formed on the lower silicon oxide film, and an upper silicon oxide film formed on the silicon nitride film. While Dobuzinsky discloses forming the ONO multilayered insulating film for use as a capacitor dielectric layer in a dynamic random access memory (DRAM) (Dobuzinsky – col. 5, lines 14-22), the patent does not disclose using the multilayered insulating film as a dielectric between a floating gated and a control gate in a memory cell.

The Maita et al. patent (Maita) discloses a method for manufacturing a semiconductor device (figs. 1-7 and accompanying text). The semiconductor device comprises a non-volatile memory cell, wherein the memory cell comprises a floating gate (fig. 3 and col. 4, lines 61-67), a control gate 38a (fig. 7 and col. 6, line 66 – col. 7, line 5), and an ONO multilayered insulating film between the floating gate and control gate (fig. 4 and col. 4, line 67 – col. 5, line 22). The ONO multilayered insulating film forms an interpoly dielectric layer (col. 5, lines 19-22).

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify the combination of Dobuzinsky, Chua, and Weimer by using the ONO multilayered insulating film as a dielectric between a floating gated and a control gate in a memory cell, as taught by Maita; because,

in addition to capacitor dielectrics in DRAM devices, ONO multilayered insulating films are also used as interpoly dielectrics in non-volatile memories.

Allowable Subject Matter

6. Claims 6, 7, 10, and 11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claims 3, 4, 8, 9, 39, and 40 are allowable.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toniae M. Thomas whose telephone number is (571) 272-1846. The examiner can normally be reached on Monday-Thursday from 8:30 a.m. to 5:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TMT
14 April 2005

Mary Wilczewski
Primary Examiner